

REMARKS

With respect to the "information disclosure statement filed 6/29/99," there is no explanation in the Office Action as to why this Information Disclosure Statement fails to comply with the Rules of Practice. Paragraph 1 of the Office Action sets forth the requirements of 37 CFR 1.98(a)(2) but does not set forth which requirement or requirements of the Rules of Practice have not been satisfied. The Examiner is requested to specify how this Information Disclosure Statement falls short of the requirements of the Rules of Practice or take into consideration, in the course of examination of this application, the references that are identified in the Information Disclosure Statement.

The Abstract has been amended so that it is now in two sentences. The only criticism of the original Abstract was that "it should not be one sentence." The amendment of the Abstract overcomes the objection to the Abstract set forth in Paragraph 3 of the Office Action.

The specification has been amended to make reference to substrate 260 that is illustrated in Figure 4. This overcomes the objection to the drawings set forth in Paragraph 4 of the Office Action.

Reconsideration and allowance of claims 1, 2, 8, and 48, "rejected under 35 U.S.C. 102(b) as being anticipated by Jensen US Patent No. 4,318,954," are respectfully requested. Referring to claim 1, the Examiner has equated:

- Applicants' substrate layer to adhesive 14 of Jensen
- Applicants' non-conductive layer to printed wiring board 13 of Jensen
- Applicants' electrically conductive circuitry to conducting strips 16 of Jensen

Considering adhesive 14 of Jensen as a "substrate layer comprising impregnated glass fibers" (see claim 1) is improper for two reasons:

(1) An adhesive, particularly the adhesive in Jensen, is not thought of as a substrate to those skilled in the art of printed circuit boards. According to *The New IEEE Standard Dictionary of Electrical and Electronics Terms*, Fifth Edition, the term "substrate," when used in the context of integrated circuits, means

"the supporting material upon or within which an integrated circuit is fabricated or to which an integrated circuit is attached"

In the field of the present invention, substrate connotes a "support" structure. The adhesive in Jensen is by no means a "support" for anything. Rather, the adhesive in Jensen must be sufficiently thin and pliable to permit the mechanical characteristics of *support* member 11 (i.e., the "low coefficient of thermal expansion approaching zero" see Jensen Abstract) to greatly reduce the apparent coefficient of thermal expansion of the printed wiring board (see Jensen Abstract). An adhesive that would take on the character of a substrate (i.e., a support structure) would be so stiff and rigid that the apparent coefficient of thermal expansion of the printed wiring board would not be reduced. This would defeat the purpose of the adhesive in Jensen.

(2) There is no indication in Jensen that adhesive 14 has "impregnated glass fibers" as specified in claim 1.

Consequently, claim 1 is patentable over Jensen because Jensen neither discloses nor suggests "a substrate layer comprising impregnated glass fibers" which is called for by claim 1. Claims 2 and 8 are dependent upon claim 1 and, therefore, are patentable over Jensen for the same reason. Claim 48 calls for "a substrate comprising impregnated glass fibers" and, therefore, is patentable over Jensen for the same reason.

Reconsideration and allowance of claims 3 through 7 and 37, "rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen US Patent No. 4,318,954," are respectfully requested. Claims 3 through 7 and 37 are dependent upon claim 1 and, therefore, are patentable over Jensen for the same reason advanced above in connection with claim 1.

Furthermore, claims 3 through 7 and 37 add limitations that the Examiner acknowledges are not taught by Jensen. Claims 3 through 7 are rejected simply because the materials that are specified in these claims "are well know materials in the art." In a Section 103 rejection, the issue is not whether these materials are well know materials in the art, but whether the use of these materials in the manner specified by the claims is well known in the art. The Examiner is requested to cite prior art that discloses the use of the materials specified by claims 3 through 7 as a "dielectric material free of continuous glass fibers" that makes it obvious to use such materials in the non-conductive layer of Applicants' invention.

With respect to claim 37, the rejection of this claim, according to the Examiner, is dependent on a showing that "the general conditions of the claim are disclosed in the prior art." With a lack of such a showing, the rejection of claim 37 should be withdrawn.

Reconsideration and allowance of claims 10, 12 through 14, 19 through 23, and 38, "rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen US Patent No. 4,318,954 in view of Applicants' Admitted prior art," are respectfully requested. Claims 10, 12 through 14, 19 through 23, and 38 are dependent upon claim 48 and, therefore, are patentable over Jensen considered alone for the same reason advanced above in connection with claim 48. Applicants' Admitted prior art does not make up for the deficiency of Jensen relative to claim 48.

Furthermore, the Examiner has failed to support the contention of obviousness of combining Jensen and Applicants' Admitted prior art in the Section 103(a) rejection of claims 10, 12 through 14, and 19 through 23. The Examiner has simply identified an element, feature or detail that is

lacking in Jensen and has concluded that when the element, feature or detail that is lacking in Jensen might be found in Applicants' Admitted prior art, Applicants' Admitted prior art can be combined with Jensen in an obvious manner solely on the basis that the element, feature or detail that is lacking in Jensen might be found in Applicants' Admitted prior art. A contention that it would have been obvious, at the time Applicants' invention was made, to combine Jensen and Applicants' Admitted prior art must be supported by a teaching or a suggestion in the prior art taken as a whole of the combination. Simply identifying the presence of the various elements, features and details of a claim in the prior art taken as a whole is insufficient to support a rejection under Section 103. The mere presence in the prior art of the elements, features and details of a patent claim does not by itself make obvious the combination of these elements, features and details.

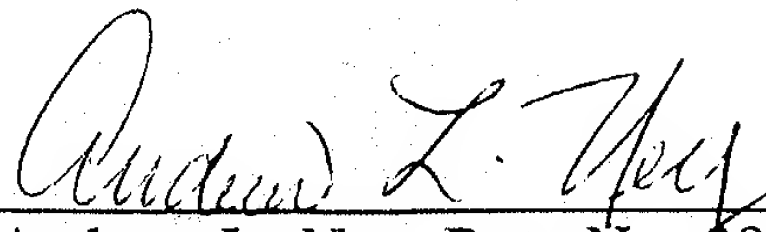
With respect to claim 38, the rejection of this claim, according to the Examiner, is dependent on a showing that "the general conditions of the claim are disclosed in the prior art." With a lack of such a showing, the rejection of claim 38 should be withdrawn.

Although claim 15 was included in the group of rejected claims in the Office Action Summary, claim 15 has not been included in the rejections based on prior art in the body of the Office Action. Consequently, Applicants assume that the Examiner erred in failing to specify on the Office Action Summary that claim 15 was either "allowed" or "objected to" and have treated claim 15 as patentable over the prior art cited by the Examiner.

In view of the foregoing amendments and remarks, this application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

RATNER & PRESTIA



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ALN/img

Attachment: Version with Markings to Show Changes Made

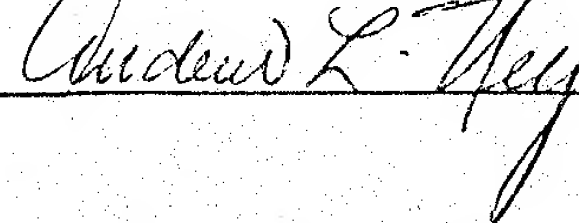
Dated: November 12, 2001

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*November 12, 2001*





VERSION WITH MARKINGS TO SHOW CHANGES MADEIN THE SPECIFICATION:

Specification at page 6, line 32 through page 7, line 8:

Referring now to Figure 4, wherein like reference numerals indicate like or similar components, a non-conductive layer 256 comprising a dielectric material free of continuous glass fibers, such as the glass-free dielectric as described above, is laminated to first surface 220 of substrate 214. A power plane 234 is disposed below substrate 214 and a second substrate 260 is disposed below power plane 234. Conductive pad 262 of plated through hole 224 is formed on top of non-conductive layer 256. Additionally electrically conductive circuitry 218 is formed on top of non-conductive layer 256. Circuitry 218 may include trace lines, pads or the like. In this manner, non-conductive layer 256 prevents glass fibers contained in substrate 214 from causing shorts between trace lines or between circuitry 218 and pad 262 or between other circuitry contained within electrically conductive circuitry 218. In addition to the previously cited materials, resin coated copper foils, such as Allied Signal Companies' "RCC" material, may be used to form layer 256 and the circuitry 262 and 218.

IN THE ABSTRACT

A printed circuit board for use in an electronic device package such as a ball grid array package or organic chip carrier package. This printed circuit board includes a glass-free dielectric for separating and insulating power cores, circuitry or plated through holes from each other to prevent shorts caused by a migration of conductive material along glass-based prepreg substrates.

B1  
concluded

dielectric as described above, is laminated to first surface 220 of substrate 214. A power plane 234 is disposed below substrate 214 and a second substrate 260 is disposed below power plane 234. Conductive pad 262 of plated through hole 224 is formed on top of non-conductive layer 256. Additionally electrically conductive circuitry 218 is formed on top of non-conductive layer 256. Circuitry 218 may include trace lines, pads or the like. In this manner, non-conductive layer 256 prevents glass fibers contained in substrate 214 from causing shorts between trace lines or between circuitry 218 and pad 262 or between other circuitry contained within electrically conductive circuitry 218. In addition to the previously cited materials, resin coated copper foils, such as Allied Signal Companies' "RCC" material, may be used to form layer 256 and the circuitry 262 and 218.

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IN THE ABSTRACT:

Please replace the abstract with the following amended abstract:

B2

A printed circuit board for use in an electronic device package such as a ball grid array package or organic chip carrier package. This printed circuit board includes a glass-free dielectric for separating and insulating power cores, circuitry or plated through holes from each other to prevent shorts caused by a migration of conductive material along glass-based prepreg substrates.

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